What is claimed is:

1. A stacked gate flash memory cell having two symmetrical memory structures therein, comprising:

a substrate having a trench therein;

a conductive layer disposed on the bottom of the trench;

a pair of source regions, each disposed in the substrate adjacent to one sidewall of the trench, electrically connecting the conductive layer;

a source isolation layer disposed on the conductive layer;

a pair of tunnel oxide layers, respectively disposed on one sidewall of the trench, contacting the source regions thereby;

a pair of floating gates, respectively disposed on the source isolation layer, contacting the tunnel oxide layers thereby;

a pair of inter-gate dielectric layers, respectively overlying the floating gate thereby;

a pair of control gates, respectively overlying the inter-gate dielectric layer thereby;

an insulating layer disposed in the trench, isolating the two control gates, forming two symmetrical memory structures therein; and

a drain region disposed in the substrate adjacent to the trench.

2. The flash memory cell as claimed in claim 1, wherein the substrate is P-type silicon substrate.

3. The flash memory cell as claimed in claim 1, wherein a bottom insulating layer is further disposed under the conductive layer.

4. The flash memory cell as claimed in claim 3, wherein the bottom insulating layer is silicon dioxide.

5. The flash memory cell as claimed in claim 1, wherein the conductive layer is N-type dopant doped polysilicon.

6. The flash memory cell as claimed in claim 1, wherein the source isolation layer is silicon dioxide.

7. The flash memory cell as claimed in claim 1, wherein the tunnel oxide layer is silicon dioxide.

8. The flash memory cell as claimed in claim 1, wherein the floating gate is N-type dopant doped polysilicon.

9. The flash memory cell as claimed in claim 1, wherein the floating gate is a composite polysilicon layer composed of a second polysilicon layer and a third polysilicon layer.

10. The flash memory cell as claimed in claim 1, wherein the floating gate is L-shaped or reverse L-shaped (⌋).

11. The flash memory cell as claimed in claim 1, wherein the inter-gate dielectric layer is silicon dioxide.

12. The flash memory cell as claimed in claim 1, wherein the control gate is N-type dopant doped polysilicon.

13. The flash memory cell as claimed in claim 1, wherein the conductive layer is composed of a polysilicon layer adjacent to sidewalls of the trench and a source line material layer in the trench.

14. A method of fabricating stacked gate flash memory cells, comprising the steps of:

providing a substrate;

forming a plurality of parallel long trenches along a first direction in the substrate;

forming a conductive layer and a pair of source regions on the bottom of each long trench, wherein the source regions are respectively disposed in the substrate adjacent to two sidewalls of each long trench and electrically connected to the conductive layer;

forming a source isolation layer on each conductive layer;

forming a tunnel oxide layer on two sidewalls of each long trench, contacting the source region thereby;

forming a pair of floating gates on the source isolation layer, respectively contacting the tunnel oxide layer;

forming a pair of inter-gate dielectric layers, respectively overlying the floating gate;

forming a pair of control gates, respectively overlying the inter-gate dielectric layer;

forming a second insulating layer in each long trench, isolating the control gates;

forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches; and

forming a drain region in the substrate adjacent to each cell trench.

15. The method as claimed in claim 14, wherein the first direction is perpendicular to the second direction.

16. The method as claimed in claim 14, wherein the substrate is P-type silicon substrate.

17. The method as claimed in claim 14, further comprising, before forming a plurality of parallel long trenches along a first direction in the substrate, the step of sequentially forming a pad oxide layer and a mask layer on the substrate.

18. The method as claimed in claim 17, wherein the mask layer is silicon nitride.

19. The method as claimed in claim 14, wherein the source isolation layer is sequentially formed by LPCVD and HDPCVD.

20. The method as claimed in claim 14, further comprising, before forming a conductive layer and a pair of source regions on the bottom of each long trench, the step of forming a bottom insulating layer in the bottom of each long trench.

21. The method as claimed in claim 14, wherein forming a conductive layer and a pair of source regions on the bottom of each long trench further comprises the steps of:

forming a source line material layer in each long trench, exposing portions of the bottom insulating layer therein;

removing the exposed bottom insulating layer, partially exposing the sidewalls of each long trench;

forming a first spacer on the sidewalls of each long trench;

etching the source line material layer, exposing portions of the bottom insulating layer adjacent to sidewalls of each long trench;

removing the exposed bottom insulating layer, respectively forming a first sidewall gap on the sidewalls of each long trench;

conformally depositing a polysilicon layer in each long trench, filling the first sidewall gaps;

performing a thermal annealing process, forming a pair of source regions in the substrate adjacent to two sidewalls of each long trench; and

etching the polysilicon layer, leaving portions of the polysilicon layer in the first sidewall gaps adjacent to the source line material layer, forming a conductive layer composed of the source material layer and the adjacent polysilicon layers in each long trench, wherein the source regions are electrically connected with the conductive layer.

22. The method as claimed in claim 21, wherein the method for depositing the source line material layer is chemical vapor deposition (CVD).

23. The method as claimed in claim 21, wherein the method for removing the exposed bottom insulating layer is wet etching.

24. The method as claimed in claim 14, further comprising, before forming a tunnel oxide layer on two sidewalls of each long trench, the step of performing a threshold voltage implantation on the sidewalls of each long trench.

25. The method as claimed in claim 14, wherein forming a pair of floating gates on the source isolation layer, and thereby respectively contacting the tunnel oxide layer further comprises the steps of:

conformally depositing a second polysilicon layer in each long trench, contacting the tunnel oxide layers therein;

forming a protective layer in each long trench, exposing portions of the second polysilicon layer;

removing portions of the second polysilicon layer exposed by the protective layer, forming a U-shaped second polysilicon layer therein;

forming a pair of second spacers, respectively disposed on the vertical portions of the U-shaped second polysilicon layer;

removing the protecting layer;

conformally depositing a third polysilcon layer in each long trench; and

etching the third polysilicon layer and the U-shaped second polysilicon layer until the source isolation layer is exposed, leaving a composite polysilicon layer composed of the second polysilicon layer and the third polysilicon layer on the two sides of the long trench as a floating gate, wherein the floating gate is L-shaped or reverse L-shaped (⌋).

26. The method as claimed in claim 25, wherein the protecting layer is boro-silicate-glass (BSG).

27. The method as claimed in claim 25, wherein the method for depositing the second spacers is LPCVD.

28. The method as claimed in claim 25, wherein the second spacer is silicon dioxide.

29. The method as claimed in claim 14, wherein forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches, further comprises the steps of:

sequentially performing photolithography and etching, defining a plurality of parallel long isolation trenches along a second direction, stopping at the conductive layer therein; and

forming an third insulating layer in each long isolation trench.

30. The method as claimed in claim 29, wherein the third insulating layer is silicon dioxide.

31. The method as claimed in claim 29, wherein the method of forming the third insulating layer is low pressure chemical vapor deposition (LPCVD).

32. The method as claimed in claim 14, wherein forming a drain region in the substrate adjacent to each of the cell trenches further comprises the steps of:

removing the mask layer and the pad oxide layer, exposing a plurality of active areas on the substrate;

performing a drain implantation on the active areas;

performing a thermal annealing process, forming a drain region in the substrate adjacent each cell trench; and

forming a fourth insulating layer on each drain region.

33. The method as claimed in claim 32, wherein impurities used in the drain region implantation are N-type impurities.

34. The method as claimed in claim 33, wherein the N-type impurities comprise arsenic (As) ions.

35. The method as claimed in claim 32, wherein the thermal annealing process is rapid thermal annealing (RTA) process.

36. The method as claimed in claim 32, wherein the fourth insulating layer is a silicon dioxide layer.

37. The method as claimed in claim 32, the method for forming the fourth insulating layer is high density plasma chemical vapor deposition (HDP CVD).